REMARKS

The present response is intended to be fully responsive to all points raised by the Examiner in the Office Action and is believed to place the application in condition for allowance. Favorable reconsideration and allowance of the application is respectfully requested.

The Applicant expresses appreciation to Examiners Shambhavi Patel and Kamini Shah for the courtesy of an interview, which was granted to the Applicant's representative, Sanford T. Colb (Reg. No. 26,856). The interview was held at the USPTO on August 12, 2009. The substance of the interview is set forth in the Interview Summary.

The application as examined includes claims 27 – 38, 40 – 51, and 71 – 78. In the present response, claims 27, 30 – 32, 34, 36, 42 – 43, and 48 – 49 are amended. Claims 1 – 26, 39, and 52 – 70 were previously canceled. Claims 28 – 29, 33, 35, 37 – 38, 40 – 41, 44 – 47, 50 – 51, and 71 – 78 are unchanged. No additional claims are canceled, and no new claims are added.

Support for amendments to the claims is set forth hereinbelow, with reference to the application as published in U.S. Patent Application Publication No. 2003/0130831:

The claimed feature recited in amended claim 27 as "a set of value-lists, each value-list thereof containing permissible values of said resource" and in amended claims 42 and 49 as "a value-list containing permissible values of a resource" is disclosed *inter alia* in paragraphs **[0019]** through **[0021]**.

The claimed feature recited in amended claims 27, 42 and 49 as "creating, by the computer executing said test program, a set of tagged value-lists by tagging members of a list of predicted results with a combination identifier identifying a particular outcome of said test program" and the claimed feature recited in amended claim 27 as "replacing said set of value-lists by said set of tagged value-lists" and in amended claims 42 and 49 as "replacing said value-list by said tagged value-list" are disclosed in paragraph **[0227]** as follows:

> **[0227]** 'Listing 4 shows that there may be dependencies between non-adjacent resources and even among resources of different types, i.e.,

memory and registers. In order to express such dependencies the syntax of the result card of results section 42 (FIG. 2) can be changed to add yet another syntactic option, as follows. *A data structure is defined which includes a combination identifier (combination-id) and a value-list. The data structure is referred to herein as a "tagged value-list". The term "combination-id" is an identifier, e.g., a string of literals, which identifies a particular outcome of the test.* The value-list associated the combination-id represents an allowed subcombination of results, as has been disclosed above. The result syntax is now modified as follows. *The set of value-lists is replaced by a set of tagged value-lists (set-of-tagged-value-lists).*' (emphasis added)

The claimed features recited in amended claims 27 and 42, respectively, as "validating the processor design if a content of said resource is equal to a member of one of said set of tagged value-lists" and "verifying the architecture if a content of said resource is equal to a member of one of said set of tagged value-lists" are disclosed *inter alia* in paragraphs **[0033]** and **[0041]** as follows:

[0033] "According to a further aspect of the method, the list of predicted resource results includes predicted results of mutually dependent non-adjacent resources. The method includes identifying a combination of the mutually dependent non-adjacent resources by tagging corresponding members of a value-list of predicted resource results with a unique combination identifier. *Verifying the actual resource result is performed by verifying that resources of the combination have actual results that are equal to a member of a corresponding one of the commonly tagged value-lists.*" (emphasis added)

[0041] "According to an additional aspect of the computer software product, the list of predicted resource results includes predicted results of mutually dependent non-adjacent resources. The method includes *identifying a combination of the mutually dependent non-adjacent resources by tagging corresponding members of the list of predicted*

> *resource results with a unique combination identifier*, and *verifying the actual resource result is performed by verifying that resources of the combination have actual results that are equal to a member of a corresponding one of the commonly tagged value-lists.*" (emphasis added)

The Applicant notes that the following terms used in the claims are defined in the application:

"value-list" — defined in paragraph **[0186]**:

> 'Here the term *"value-list"* refers to a hyphen-separated list of values, each element of which corresponds respectively to the value of the resource identified in the resource-id of the result card and its succeeding adjacent resources.'

"combination identifier" ("combination-id") — defined in paragraph **[0227]**:

> 'The term "combination-id" is an identifier, e.g., a string of literals, which identifies a particular outcome of the test.'

"tagged value-list" — defined in paragraph **[0227]**:

> 'A data structure is defined which includes a combination identifier (combination-id) and a value-list. The data structure is referred to herein as a "tagged value-list" '

Claims 27 – 38, and 40 – 51 stand rejected under 35 U.S.C. §102(b) as being anticipated by Genesys-MP User's Guide ("Genie").

Claims 71 – 78 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Genie in view of "Development and Validation of a Hierarchical Memory Model Incorporating CPU and Memory-Overlap" ("Luo").

The present invention provides a computer program product for validating a processor design by simulating program execution for a test program having at least two simulated processes which access mutually-dependent non-adjacent resources, and by creating one or more tagged value-lists incorporating a set of non-unique values associated with a combination identifier identifying a particular outcome of the test program. The contents of the resources are then compared with the non-

unique values in the tagged value-lists to validate the processor design for the test program.

Genie describes the use and operation of the "Genesys" multiprocessor test system.

Luo describes a "memory-centric" model for use in analyzing and characterizing multiprocessor computer systems.

At the interview, the independent claims were discussed regarding clarification. The Interview Summary states, in relevant part:

> 'After reviewing the proposed amendments, Examiner and Applicant's representative agreed that the claims need to be amended, as they require clarification regarding the following issues: 1. lack of antecedent basis, particularly "set of list of values" (see claim 30) 2. use of outcome of test program in creating the tagged value-list 3. result achieved by use of tagged-value list. Examiner noted that the recitation "may be accessed" should be made more definite. Applicant's representative noted that amended features do not appear to be in the prior art and Examiner noted that this can only be determined upon review of the filed claimed amendments.'

Regarding clarification of the claims as described in the Interview Summary:

> The Applicant is amending claims 27 and 30 to provide a clear antecedent basis. In place of "set of list of values" amended claim 27 recites "a set of value-lists" and claim 30 recites "said set of value-lists". Support in the specification for "set of value-lists" is found *inter alia* in paragraphs **[0019]** and **[0185]**. Applicant is also amending claims 31 – 32, 34, 43 and 48 to provide proper antecedent basis for all elements recited therein in light of the amendments to the independent claims from which they depend. Applicant is also amending claim 36 to ensure proper antecedent basis for all elements recited therein.
>
> The Applicant is amending independent claims 27, 42, and 49 to clarify the use of the outcome of the test program in creating the

tagged value-list, by reciting "creating, by the computer executing said test program, a tagged value-list ... wherein said creating said tagged value-list comprises tagging members of a list of predicted results with said combination identifier". As previously noted, support for the above is found in paragraph [0227] of the specification.

The Applicant is amending independent claims 27 and 42 to clarify the result achieved by the value-lists, by reciting "validating the processor design if a content of said resource is equal to a member of one of said set of tagged value-lists" and "verifying the architecture if a content of said resource is equal to a member of one of said set of tagged value-lists". As noted previously, this is supported in paragraph [0033] of the specification.

The Applicant is amending claim 27 to recite "accessed" in place of "may be accessed" in keeping with the Examiner's note to make the recitation more definite.

The Applicant is overcoming the 35 U.S.C. §102(b) rejection by amending independent claims 27, 42, and 49 to recite novel features of the invention which are neither disclosed nor reasonably suggested by the cited prior art. The Applicant respectfully submits that the cited prior art references, individually as well as in combination, fail to show or suggest at least the following features recited in amended independent claims 27, 42, and 49:

creating, by the computer executing said test program, a tagged value-list comprising said set of non-unique values and a combination identifier identifying a particular outcome of said test program;

replacing a set of lists of values by a set of tagged value-lists; and

validating the processor design if a content of said resource is equal to a member of one of said set of tagged value-lists.

The Applicant therefore respectfully submits that amended independent claims 27, 42, and 49 are patentable over the art of record. Each of the remaining claims depend directly or ultimately from one of the amended independent claims, and therefore are also allowable over the art of record.

In view of the foregoing remarks, all of the claims are believed to be in condition for allowance. Favorable reconsideration and allowance of the application is respectfully requested.

Please charge any fees associated with this response to Deposit Account 09-0468.

Respectfully submitted,

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